UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,657	06/12/2006	Ari Pekkarinen	915-001.087	1500

4955 7590 10/20/2009

WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
CHEN, XIAOLIANG	
ART UNIT	**PAPER NUMBER**
2841	
MAIL DATE	**DELIVERY MODE**
10/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,657	PEKKARINEN ET AL.	
	Examiner	Art Unit	
	Xiaoliang Chen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06-12-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgement is made of Preliminary Amendment filed 06-12-09.

2. Claims 1-14 and 16-20 are amended.

3. Claim 15 is canceled.

4. Claims 21 and 22 are added.

5. Specification is amended.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 4, 10 and 14 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4, recites the limitation "a layer of electroconductive material", the same limitation already in claim 3, on which claim 4 is depended.

Claim 10, recites the limitation "a layer of electroconductive material", the same limitation already in claim 9, on which claim 10 is depended.

Claim 14, recites the limitations "a light emitting diode" and "a photoconductive layer", the same limitations already in claim 7, on which claim 14 is depended.

8. **Claim 14 is rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14, recites the limitation "the keypad", and there is insufficient antecedent basis for this limitation in the claim, since there is no limitation “a keypad” anywhere before.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-13 and 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamada et al. (US6331063).

Re Claim 1, Kamada et al. show and disclose

An apparatus comprising:

a photoconductor (11 and 15, fig. 1) having a surface,

an electroconductive material (12, fig. 1) induced on said surface of the photoconductor, which material is connectable to a ground plane (a plating ground layer [col. 3, line 61]) in order to conduct electrostatic discharges through the electroconductive material to the ground plane.

Re Claim 2, Kamada et al. show and disclose

The apparatus according to claim 1, wherein the photoconductor is provided with an aperture (hole for 1 in 11, fig. 1), and that the photoconductor is provided with electroconductive material at least around the edges of the aperture (fig. 1).

Re Claim 3, Kamada et al. show and disclose

The apparatus according to claim 1, wherein the electroconductive material is integrated with the photoconductor as a layer (12, fig. 1, and 19a, fig. 31) of electroconductive material that covers the whole surface of the photoconductor (fig. 1 and fig. 31).

Re Claim 4, Kamada et al. show and disclose

The apparatus according to claim 3, wherein the electroconductive material is integrated with the photoconductor as the layer of electroconductive material (19a, fig. 31) for conducting light in the photoconductor and for shielding the light source against electrostatic pulses (shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]).

Re Claim 5, Kamada et al. show and disclose

The apparatus according claim 1, wherein the electroconductive material is metal (12, fig. 1) and is connectable to the ground plane through the electroconductive material.

Re Claim 6, Kamada et al. show and disclose

The apparatus according to claim 1, wherein the electroconductive material is realized on the surface of the photoconductor by means of an

electroconductive film (metal film [col3, line 60]), or by inducing chemically or electrochemically.

Re Claim 7, Kamada et al. show and disclose

An apparatus for shielding a component against electrostatic discharge, said apparatus comprising

a light emitting diode (1, fig. 1) and a photoconductor layer (11 and 15, fig. 1) for conducting the light emitted by the light emitting diode, wherein the photoconductor layer includes electroconductive material (12, fig. 1), and that the electroconductive material is connectable to a ground plane (a plating ground layer [col. 3, line 61]) in order to conduct electrostatic discharges from the photoconductor layer to the ground plane.

Re Claim 8, Kamada et al. show and disclose

The apparatus according to claim 7, wherein the photoconductor layer is provided with an aperture (hole for placing 1 in 11, fig. 31), so that the light emitting diode is at least partly placed in the aperture (fig. 31), inside the photoconductor layer (fig. 31), and that the photoconductor layer is provided with electroconductive material at least around the edges of the aperture (fig. 31).

Re Claim 9, Kamada et al. show and disclose

The apparatus according to claim 7, wherein in the surface of the photoconductor layer there is integrated a layer of electroconductive material (19a, fig. 31), said layer covering the whole surface of the photoconductor layer.

Re Claim 10, Kamada et al. show and disclose

The apparatus according to claim 9, wherein in the surface of the photoconductor layer, there is integrated the layer of electroconductive material (19a, fig. 31) for shielding the components against electrostatic pulses (shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]) and for conducting the light emitted by the light emitting diode (1, fig. 31) in the photoconductor layer.

Re Claim 11, Kamada et al. show and disclose

The apparatus according claim 7, wherein the light emitting diode is placed on a printed circuit board (19b, fig. 31), the photoconductor layer is placed on the component side of the circuit board (fig. 31), and the electroconductive material is placed on that side of the photoconductor layer that faces away from the circuit board (fig. 31) and the electroconductive material is connectable to the ground plane (a plating ground layer [col. 3, line 61]) of the circuit board.

Re Claim 12, Kamada et al. show and disclose

The apparatus according to claim 7, wherein the electroconductive material is metal (12, fig. 1), and it is connected to the ground plane (a plating ground layer [col. 3, line 61]) by electroconductive material.

Re Claim 13, Kamada et al. show and disclose

The apparatus according to claim 7, wherein the electroconductive material is realized on the surface of the photoconductor layer by an electroconductive film (metal film [col3, line 60]), or by inducing chemically or electrochemically.

Re Claim 21, Kamada et al. show and disclose

A method comprising:

placing a light emitting diode (1, fig. 31) on a printed circuit board (19b, fig. 31),

arranging a photoconductor layer (11 and 15, fig. 31) on a component side (top) of the circuit board,

inducing an electroconductive material (12, fig. 1) to the photoconductor layer,

connecting the electroconductive material to a ground plane (a plating ground layer [col. 3, line 61]) of the circuit board in order to conduct electrostatic discharges from the photoconductor layer to the ground plane of the circuit board (shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]).

Re Claim 16, Kamada et al. show and disclose

The method according to claim 21, wherein the photoconductor layer is provided with an aperture (hole for 1 in 11, fig. 31), so that the light emitting diode placed on the circuit board is arranged at least partly in the aperture (fig. 31), inside the photoconductor layer (fig. 31), and that in the photoconductor layer, there is induced electroconductive material (12, fig. 1) at least around the edges of the aperture.

Re Claim 17, Kamada et al. show and disclose

The method according to claim 21, wherein on the outermost surface of the photoconductor layer, facing away from the circuit board (fig. 31), there is integrated a layer (12, fig. 1, and 19a, fig. 31) of electroconductive material, which layer covers the whole surface of the photoconductor layer (fig. 1 and fig. 31).

Re Claim 18, Kamada et al. show and disclose

The method according to claim 17, wherein the electroconductive material is induced for shielding components of the circuit board against electrostatic pulses (shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]) and for conducting the light emitted by the light emitting diode (1, fig. 31) of the circuit board (19b, fig. 11) in the photoconductor layer (11 and 15, fig. 31).

Re Claim 19, Kamada et al. show and disclose

The method according to claim 21, wherein the electroconductive material is metallized (plating [col. 3, line 61]) to the photoconductor layer and connected to the ground plane (a plating ground layer [col. 3, line 61]) of the circuit board by electroconductive material.

Re Claim 20, Kamada et al. show and disclose

The method according to claim 21, wherein the electroconductive material is realized in the photoconductor layer by means of an electroconductive film (metal film [col3, line 60]), or by inducing chemically or electrochemically.

Re Claim 22, Kamada et al. show and disclose

An apparatus comprising:

means for providing a photoconductor (11 and 15, fig. 1) having a surface,

means for providing an electroconductive material (12, fig. 1) induced on said surface of the means for providing a photoconductor (fig. 10), which material is connectable to a ground plane (a plating ground layer [col. 3, line 61]) in order to conduct electrostatic discharges through the means for providing an electroconductive material to the ground plane (shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamada et al. in view of Yu et al. (US7053799).

Re Claim 14, Kamada et al. show and disclose

The apparatus according to claim 7, wherein on the circuit board, there is the light emitting diode (1, fig. 31), and that the device apparatus comprises the photoconductor layer (11 and 15, fig. 31) for conducting the light emitted by the light emitting diode (1, fig. 31),

Kamada et al. does not disclose

the light emitting diode for illuminating a keypad and for conducting the light emitted by the light emitting diode to a key.

Yu et al. teaches a device wherein

the light emitting diode for illuminating a keypad and for conducting the light emitted by the light emitting diode to a key (an illuminated keypad and button [col. 3, line 31]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the LED luminaries of Kamada et al. with the transparent keypad as taught by Yu et al., in order to provide effective light illumination the transparent keypad in a dark environment (Yu et al. col. 6, line 22-52).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-7388569 US-5977718 US-5696372 US-5889308 US-6536913.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiaoliang Chen whose telephone number is (571)272-9079. The examiner can normally be reached on 8:00-5:00 (EST), Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Xiaoliang Chen/
Examiner, Art Unit 2841

Xiaoliang Chen
Examiner
Art Unit 2841